

WE CLAIM:

1. An integrated circuit chip mounted on a leadframe, said leadframe having a plurality of segments, comprising:

5 a network of power distribution lines deposited on the surface of said chip over active components of said circuit;

said lines connected vertically to said components by metal-filled vias, and also to said segments by conductors; and

10 the majority of said lines patterned as straight lines between said vias and said conductors, respectively, thereby minimizing the distance for power delivery between a selected segment and one or more corresponding active components, to which said power is to be delivered.

2. The chip according to Claim 1 further having said lines fabricated with a sheet resistance of less than 1.5 $\text{m}\Omega/\square$ and positioned to minimize parasitic electrical losses in power delivery between a selected segment and one or more corresponding active components, to which said power is to be delivered.

3. The chip according to Claim 2 wherein said parasitic electrical losses include voltage drops during said power current flow, capacitances between said network and said active components, and inductances between network lines.

4. A semiconductor device wherein electrical parasitics are minimized by individualized power distributors deposited over active integrated circuit components, comprising:

a semiconductor chip having first and second surfaces;

an integrated circuit fabricated on said first chip surface, said circuit having active components, at least one metal layer, and being protected by a mechanically strong, electrically insulating overcoat having a plurality of metal-filled vias to contact said at least one metal layer, and a plurality of windows to expose circuit contact pads;

electrically conductive films deposited on said overcoat and patterned into a network of lines substantially vertically over said active components, said films in contact with said vias and having an outermost film of non-corrodible, metallurgically attachable metal;

said network patterned to distribute power current while minimizing parasitic electrical losses between said network and said active components; said network further patterned to minimize silicon real estate consumed by power interconnections between said active components;

a leadframe having a chip mount pad, a first plurality of segments providing electrical signals, and a second plurality of segments providing electrical power and ground; said second chip surface attached to said chip mount pad;

electrical conductors connecting said chip contact pads with said first plurality of segments; and electrical conductors connecting said network lines with said second plurality of segments.

5. The device according to Claim 4 wherein said chip is selected from a group consisting of silicon, silicon germanium, gallium arsenide, and any other semiconductor material customarily used in electronic device fabrication.
6. The device according to Claim 4 wherein said circuit comprises a plurality of active and passive electronic components arranged horizontally and vertically.
7. The device according to Claim 4 wherein said integrated circuit comprises multi-layer metallization, at least one of said layers made of pure or alloyed copper, aluminum, nickel, or refractory metals.
8. The device according to Claim 4 wherein said overcoat comprises materials selected from a group consisting of silicon nitride, silicon oxynitride, silicon carbon alloys, polyimide, and sandwiched films thereof.
9. The device according to Claim 4 wherein said leadframe is pre-fabricated from a sheet-like material selected from a group consisting of copper, copper alloy, aluminum, iron-nickel alloy, or invar.
10. The device according to Claim 4 further comprising an encapsulation enclosing said chip, chip mount pad, electrical conductors, and at least portions of said leadframe segments.
11. The device according to Claim 10 wherein said encapsulation comprises a polymer compound fabricated in a transfer molding process.
12. The device according to Claim 10 wherein leadframe segment portions not included in said encapsulation are shaped as leads or pins, solderable to outside parts.
13. The device according to Claim 4 wherein said lines and contact pads are attached to outside parts by solder

balls.

14. The device according to Claim 4 wherein said conductive films comprise a stack of stress-absorbing metal films under said outermost metallurgically attachable film.

5 15. The device according to Claim 4 wherein said metallurgical attachment comprises wire ball and stitch bonding, ribbon bonding, and soldering.

10 16. The device according to Claim 14 wherein said stack of films comprise a layer of seed metal, promoting adhesion to said vias and inhibiting migration of overlying metals to said vias, at least one stress-absorbing metal layer, and an outermost metallurgically attachable metal layer.

15 17. The device according to Claim 16 wherein said seed metal is selected from a group consisting of tungsten, titanium, titanium nitride, molybdenum, chromium, and alloys thereof.

20 18. The device according to Claim 16 wherein said stress-absorbing metal layer comprises at least one layer selected from a group consisting of copper, nickel, aluminum, and alloys thereof.

25 19. The device according to Claim 16 wherein said outermost metal layer is selected from a group consisting of pure or alloyed aluminum, gold, palladium, silver and platinum.

20. The device according to Claim 4 wherein said conductors are bonding wires, bonding ribbons, or solder balls.

30 21. The device according to Claim 20 wherein said bonding wire is selected from a group consisting of pure or alloyed gold, copper, and aluminum.

22. The device according to Claim 20 wherein said solder ball is selected from a group consisting of pure tin,

tin alloys including tin/copper, tin/indium, tin/silver, tin/bismuth, tin/lead, and conductive adhesive compounds.

23. The device according to Claim 4 wherein said network of lines is electrically further connected to selected segments suitable for outside electrical contact.

24. A method for fabricating a semiconductor device including a semiconductor chip having first and second surfaces, comprising the steps of:

forming an integrated circuit on said first chip surface, said circuit including active components, at least one metal layer, and a mechanically strong, electrically insulating protective overcoat;

forming a plurality of vias through said overcoat to access said at least one metal layer;

filling said vias by depositing a stack of metal films on said overcoat, said stack having at least one stress-absorbing film and an outermost film being non-corrodible and metallurgically attachable;

patterning said films into a network of lines such that said lines are located substantially vertical over said active components, thus providing power current distribution while minimizing parasitic electrical losses between said network and said active components;

forming a plurality of windows in said overcoat to expose circuit contact pads;

providing a pre-fabricated leadframe comprising a chip mount pad, a first plurality of segments suitable for electrical signals, and a second

plurality of segments suitable for electrical power and ground;

attaching said chip to said chip mount pad;

attaching electrical conductors to said circuit

5 contact pads and said first plurality of segments; and

attaching electrical conductors to said network of lines and said second plurality of segments.

10 25. The method according to Claim 24 wherein said step of depositing said stack of metal films comprises the steps of:

depositing a seed metal film on the surface of said overcoat:

15 forming a plating pattern over said seed metal film, said plating pattern resulting in exposed portions of said seed metal film and blocking the rest of said seed metal film;

20 covering said exposed portions of said seed metal film with an electrically conductive, stress-absorbing support film;

covering said support film with a metallurgically attachable film; and

removing said blocked portions of said seed metal film.

25 26. The method according to Claim 24 wherein said steps of attaching electrical conductors to said contact pads and said network of lines comprise the step of either bonding wires or ribbons to said contact pads and network of lines, or reflowing solder balls to said
30 contact pads and network of lines.

27. The method according to Claim 26 further comprising the step of encapsulating said chip, chip mount pad,

electrical conductors and at least a portion of
said leadframe segments in a package.

28. The method according to Claim 24 further comprising the
step of attaching said circuit contact pads and said
network of lines to outside parts by solder balls.

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